AF/2814

Attorney Docket No: SEL 194

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Suzawa et al.

Serial No.: 09/615,449

Filed: July 13, 2000

For: Wiring And Manufacturing Method Thereof, Semiconductor Device Comprising Said Wiring, And Dry Etching Method

Examiner: H. Trinh

Art Unit: 2814

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

June 3, 2005

Signature Shanna Wallace

Date June 3 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE G (AFTER FINAL)

Applicants have the following response to the Final Rejection of April 4, 2005. As explained herein, Applicants respectfully submit that the Examiner's interpretation of the references is incorrect, and as a result, the rejections based on these references are incorrect and should be withdrawn.

Claim Rejections - 35 USC §103

In the Final Rejection, the Examiner now rejects Claims 43-54 and 79-112 [sic 114] under 35 USC §103 (a) as being unpatentable over Jinnai (US 6,130,119 - a new reference) in view of Meikle et al. (US 6,429,086 - a new reference). This rejection is respectfully traversed.

More specifically, independent Claims 43, 49, 79, 85, 91, 97, 103, and 109 are directed to a semiconductor device comprising a gate electrode over the semiconductor layer with a gate insulating film interposed therebetween, wherein the gate electrode comprises a first conductive layer comprising nitride (Claims 43, 79, 91, 103) or tungsten nitride (Claims 49, 85, 97, 109) and a second conductive layer comprising tungsten on the first conductive layer, and wherein a bottom surface of the first conductive layer is in contact with the gate insulating film.

In the Final Rejection, the Examiner contends that Jinnai discloses a semiconductor device "wherein the gate electrode 9 (fig. 9) may include more than one layer (col. 9, lines 12-16) constituting different materials as discloses." Applicants respectfully disagree with this interpretation of the reference.

In particular, Fig. 9 in Jinnai merely shows gate electrode 9 as a single layer. Col. 9, lns. 12-16 in Jinnai state "...a gate electrode 9 constituting of aluminum, a molybdenum-tungsten alloy, titanium *or* tantalum is formed on the upper surface of the gate insulating film 8..." (emphasis added) Hence, Jinnai does not teach a gate electrode with a plurality of layers but instead clearly disclosed a gate electrode structure with a single layer which is made of one of the 4 materials listed at col. 9, lines 12-16. The use of the word "or" at col. 9, lines 12-16 clearly indicates that the gate electrode is made of one of those materials, not a plurality of them. Therefore, the Examiner's interpretation of this reference is incorrect, and Jinnai fails to disclose or suggest this claimed feature of the present application.

In the Final Rejection, the Examiner also acknowledges that Jinnai does not disclose that a first conductive layer of the gate electrode is made of a nitride and the second conductive layer of the gate electrode is made of tungsten. As a result, the Examiner cites Meikle and contends that Meikle discloses "a semiconductor device having a substrate 150 (fig. 5), *a gate insulating*

layer 140 (fig. 5), a gate electrode having a first conductive layer 130 made from a nitride (col. 3, line 49) and a second conductive layer 135 (fig. 5) made from a tungsten (col. 3, line 50)" (emphasis added). Applicants also disagree with this interpretation of the reference.

In particular, reference numeral 140 in Fig. 5 in Meikle is directed to a "polycrystalline silicon layer 140." Col. 3, lines 49-50 in Meikle. Meikle states that layer 160 which is below layer 140 in Fig. 5 in Meikle is directed to a "gate oxide" which corresponds to a gate insulating layer. See col. 3, lines 53-54 in Meikle. Hence, Meikle discloses a gate electrode having a structure composed of a gate insulating layer 160, a first conductive layer 140 of polycrystalline silicon *formed on* the gate insulating layer 160, a second conductive layer 130 of tungsten nitride formed on the first conductive layer 140 (and not in contact with gate insulating layer 160), and a third conductive layer 135 of tungsten nitride formed on the second conductive layer 130. Therefore, Meikle does not disclose or suggest the structure of the claimed invention wherein a first conductive layer of nitride or tungsten nitride *is in contact with* the gate insulating film.

Accordingly, as explained above, when each of the cited references is properly interpreted, even if the two references are combined, the combination thereof does not disclose or suggest the claimed invention. Therefore, is respectfully requested that this rejection be withdrawn.

Withdrawal of Final Rejection

As explained above, the Final Rejection is based on an erroneous interpretation of the references. When properly interpreted, the references do not disclose or suggest the claimed invention. Accordingly, it is respectfully submitted that this Final Rejection was issued in error and should be withdrawn.

Conclusion

For at least the above-stated reasons, the claims of the present application are patentable over the cited references and should be allowed.

If the Examiner disagrees with Applicants or has any further rejections, it is requested that she call the undersigned to discuss.

If any fee should be due for this response, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: June 3, 2005

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